REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-8 remain in the application and are subject to examination. No claims have been withdrawn, amended, added or canceled herein. Claims 4-7 have been allowed.

In "Claim Rejections - 35 USC § 102" on pages 2-6 of the above-identified Office Action, claims 1-3 and 8 have been rejected as being fully anticipated by U.S. Patent No. 5,627,092 to Alsmeier et al. (hereinafter Alsmeier) under 35 U.S.C. § 102(b).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method for fabricating a buried bit line for a semiconductor memory, which comprises:

providing a semiconductor body;

applying a lower boundary layer and a storage layer to the semiconductor body;

applying a sacrificial layer made from a material selectively etchable with respect to the storage layer and to polysilicon onto the storage layer;

producing openings in the sacrificial layer, the storage layer, and the lower boundary layer, extending to the semiconductor body, the openings being produced above regions where buried bit lines are to be produced;

introducing doped polysilicon into the openings;

etching back the polysilicon to a residual portion;

removing the sacrificial layer;

applying an upper boundary layer on a surface of the storage layer and the residual portion of the polysilicon and oxidizing the residual portion of the polysilicon to form an oxide region, the oxide region being thicker than the lower boundary layer, the lower boundary layer, the storage layer and the upper boundary layer acting as a gate dielectric;

forming a diffusion region in the semiconductor body below the oxide region during the oxidation of the residual portion of the polysilicon, the diffusion region forming the buried bit line.

The Alsmeier reference discloses a deep trench DRAM process on SOI for a low-leakage DRAM cell. The Examiner's efforts in carefully comparing the features taught by Alsmeier to the limitations of the claims of the instant application are appreciated. However, in order to be able to reject a claim under 35 USC § 102 every limitation of the claim must be shown in the reference. It is respectfully believed that the Examiner's description of the Alsmeier method and therefore

the comparison to the limitations of the claims of the instant application, is faulty. Accordingly, as will be explained below, it is believed that claims 1-3 and 8 are allowable over Alsmeier in their previous form.

The method of Alsmeier does not produce a storage layer

The Examiner has stated on page 3 of the Office action that Alsmeier applies a storage layer 50 to a semiconductor substrate 36. However, it can be seen from Fig. 4.8 of Alsmeier that the pad nitride layers 50 are removed. That is also explicitly stated in the corresponding description in the first paragraph of column 4 of the reference. Therefore, the pad nitride layer portions 50 of Alsmeier cannot be compared to the storage layer recited in claim 1 of the instant application. A storage layer is understood to be a layer where charges are trapped or stored. Therefore, even if the pad nitride layer portions 50 of Alsmeier were formed of the same material as the storage layer of the claims of the instant application, the pad nitride layer portions 50 of Alsmeier cannot be a storage layer since the pad nitride layer portions 50 of Alsmeier are not present in the final device. The method of fabricating a buried bit line recited in claim 1 of the instant application requires a storage layer to be present in the completed device.

The method of Alsmeier does not produce openings extending to the semiconductor body and above regions where buried bit lines are to be produced nor an oxide region being thicker than the lower boundary layer

The Examiner has stated on page 3 of the Office action that the method of Alsmeier produces openings 44, 46 extending to the semiconductor body 36 and above regions where buried bitlines are to be produced. However, openings 44, 46 produced by the method of Alsmeier do not only extend to the semiconductor body 36, but instead form deep recesses within the semiconductor body.

The openings are also not produced above regions where buried bitlines are to be produced. There are no lower bitlines underneath the openings 44 and 46, which are provided for storage in the completely different DRAM structure produced by Alsmeier, which has nothing to do with the production of buried bitlines.

The oxide layer which is produced by a thermal oxidation of the polysilicon that is previously introduced into the openings is shown in Fig. 4.7. It is certainly incomparably thinner than the layer which is identified as the lower boundary layer by the Examiner. Thus, there is no oxidized region which is thicker than the lower boundary layer in the

method of Alsmeier.

The method of Alsmeier does not form a diffusion region in the semiconductor body, below the oxide region, forming the buried bit line

The Examiner has stated on page 5 of the Office action that Alsmeier discloses in column 3, lines 56-65 thereof the step of forming a diffusion region in the semiconductor body below the oxide region during the oxidation of the residual portion of the polysilicon, the diffusion region forming the buried bitline. However, the so-called buried straps 56 of Alsmeier are formed in the silicon device layer portions 42, which is the silicon body layer of an SOI structure and does not form a part of the bulk substrate. Therefore, the buried straps 56 do not form diffusion regions in the semiconductor body below the oxide regions and thus do not form buried bitlines.

Clearly, Alsmeier does not show producing a storage layer, producing openings extending to a semiconductor body and above regions where buried bitlines are to be produced, producing an oxidized region which is thicker than the lower boundary layer, nor forming a diffusion region in the semiconductor body, below the oxide region, forming the buried bitline, as recited in claim 1 of the instant application.

It is accordingly believed to be clear that neither Alsmeier nor any of the other references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims 2, 3 and 8 are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-3 and 8 and the issuance of a Notice of Allowance for claims 1-8, are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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LAG/am

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